

10/038,340

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,750,547 B2
DATED : June 15, 2004
INVENTOR(S) : Boon Suan Jeung et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page.

Item [56], **References Cited, OTHER PUBLICATIONS**, please insert
-- US Application No. 09/981,948 Boon et al. Filed 10/16/01 --; and please delete
the second occurrence of "EPIC CSP™ Chip Scale Package Technology, "Low
Cost Area Array Package Fully Integrates Printed Circuit, Chip Interconnect and
Assembly," EPIC Technologies, Inc., 30 pages.";

Signed and Sealed this

Nineteenth Day of April, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office